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09/978,018	10/17/2001	Hideki Takauchi	100021-00062	3806

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EXAMINER	
NGUYEN, MINH T	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/978,018	Applicant(s) TAKAUCHI ET AL.	
	Examiner Minh Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on 7/23/02 has been received and entered in the case. The amendment presented therein overcomes the some of the indefiniteness rejections and informality objections, and therefore, are withdrawn. New grounds of rejections necessitated by the amendment are set forth below. This action is FINAL.

Drawings

2. An attached copy of the drawing corrections to Figs. 1 and 2 is not seen in the response even though it is noted in the response. Figures 1-2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 9 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim, or amend the claim to place the claim in proper dependent form, or rewrite the claim in independent form. Replacing the first and third transistors by a common transistor as recited in claim 9 is not seen as further limit claim 3.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6-9 and 15-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 6, "said first and second transistors" recited on line 2 lack antecedent basis. For further examination, it is assumed that it is referring to the first and second transistors in the first termination resistor block. "said first termination resistor blocks" recited on line 3 lacks antecedent basis, i.e., there is only one "first termination resistor block" in claim 3 and 4, "said plurality of first termination resistor blocks" recited on line 3 lacks antecedent basis.

As per claim 7, "said third and fourth transistors" recited on line 2 lacks antecedent basis.

As per claim 8, "said third and fourth transistors" recited on line 1 lacks antecedent basis. For further examination, it is assumed that it is referring to the third and fourth transistors in the second termination resistor block. "said second termination resistor blocks" recited on line 3 lacks antecedent basis, i.e., there is only one "second termination resistor block" in claim 3 and 4, "said plurality of second termination resistor blocks" recited on line 3 lacks antecedent basis.

As per claim 9, "said first transistor and said third transistor" recited on line 2 lacks antecedent basis.

As per claim 15, the same problems exist as discussed in claim 6.

As per claim 16, the same problem exists as discussed in claim 7.

As per claim 17, the same problems exist as discussed in claim 8.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-6, 8-15 and 17-23 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,026,456 to Ilkbahar.

As per claim 1, Ilkbahar discloses a termination resistor circuit (Fig. 5), provided in an interface circuit (Fig. 2) through which signals are transferred (Fig. 2, the signals are transferred on the bus 205), comprising:

a first termination resistor block (the first block comprises transistors 542 and 544) having a plurality of transistors (transistors 542 and 544, i.e., more than one) with the same logic voltage being applied to gates of the transistors (the gates of transistors 542 and 544 both receive the voltage on line 524) of the first termination resistor block; and

a second termination resistor block (the second block comprises transistors 560 and 532) having a plurality of transistors (transistors 560 and 532) with different logic voltages being applied to gates of the transistors (the logic voltage applied on line 528 to the gate of transistor 560 can be different from the logic voltage applied on line 526 to the gate of transistor 532),

which differs in configuration from the first termination resistor block (transistor 560 is NMOS and transistor 532 is PMOS whereas transistors 542 and 544 are PMOSs, i.e., different configurations);

the limitation recited on the last two lines is met because they are controlled by different control signals.

As per claim 2, transistors 542 and 544 in the first termination resistor block are PMOSs, i.e., same conductivity type, and in the second termination resistor block, transistor 560 is NMOS and transistor 532 is PMOS i.e., different conductivity types.

As per claim 3, Ilkbahar discloses a termination resistor circuit (Fig. 5), provided in an interface circuit (Fig. 2) through which signals are transferred (Fig. 2, the signals are transferred on the bus 205), comprising:

a first termination resistor block (the first block comprises transistors 542 and 544) having a plurality of transistors (transistors 542 and 544, i.e., more than one), the limitation that a gate of at least one of the transistors of the first termination resistor block being applied with a supply voltage or a voltage of the transmission line is met because the line 524 which is connected to the gates of transistors 542 and 544 can receive any voltage which includes the voltage of the supply voltage or a voltage of the transmission line; and

a second termination resistor block (the second block comprises transistors 560 and 532) having a plurality of transistors (transistors 560 and 532) with different logic voltages being applied to gates of the transistors (the logic voltage applied on line 528 to the gate of transistor 560 can be different from the logic voltage applied on line 526 to the gate of transistor 532), which differs in configuration from the first termination resistor block (transistor 560 is NMOS

and transistor 532 is PMOS whereas transistors 542 and 544 are PMOSs, i.e., different configurations);

the limitation recited on the last two lines is met because they are controlled by different control signals.

As per claim 4, this claim is rejected for the same reason noted in claim 2.

As per claim 5, Ilkbahar discloses a termination resistor circuit (Fig. 5), provided in an interface circuit (Fig. 2) through which signals are transferred (Fig. 2, the signals are transferred on the bus 205), comprising:

a first termination resistor block (the first block comprises transistors 542 and 544) having a plurality of transistors (transistors 542 and 544, i.e., more than one) of the same conductivity type (both are PMOS); and

a second termination resistor block (the second block comprises transistors 560 and 532) having a plurality of transistors (transistors 560 and 532), which differs in configuration from the first termination resistor block (transistor 560 is NMOS and transistor 532 is PMOS whereas transistors 542 and 544 are PMOSs, i.e., different configurations);

the limitation that the first termination resistor block operates and maintains a specific resistance value when a value of the transmission line is near a supply voltage is met because when the voltage applied to the gates of transistors 542 and 544 is unchanged when a value of the transmission line is near a supply voltage, the transistors 542 and 544 has a specific resistance value;

the limitation that the second termination resistor block comprises a first conductivity type and a second conductivity type reads on transistor 560 (PMOS) and transistor 532(NMOS),

respectively, the limitation that the first conductivity type transistor does not operate near a first supply voltage and the second conductivity type transistor does not operate near a second supply voltage is met because transistors 560 and 532 have the structure which can perform the recited function; and

the limitation recited on the last two lines is met because they are controlled by different control signals.

As per claim 6, the limitation recited in the claim is always met since the specific sizes of transistors 542 and 544 are chosen to have the specific chosen weights.

As per claim 8, the limitation recited in the claim is always met since the specific sizes of transistors 560 and 532 are chosen to have the specific chosen weights.

As per claim 9, Ilkbahar further discloses the termination resistor circuit comprises a first termination resistor block (transistors 532 and 534) and a second termination resistor block (transistors 560 and 532). It is clear that the grouping of the first and second termination resistor blocks satisfies the limitation recited in the claim since transistors 532 and 534 are of the same type and transistors 560 and 532 are of different type, and transistor 532 is the recited common transistor.

As per claim 10, this claim is rejected for the same reasons noted in claim 1, and further, the recited signal transmission system is disclosed in Fig. 2, the recited transmitting circuit reads on the output driver 212, the recited transmission line reads on the bus 205, and the recited termination resistor circuit reads on the circuit 242 which is provided in the interface circuit 240.

As per claim 11, this claim is rejected for the same reason noted in claim 2.

As per claim 12, Ilkbahar discloses a signal transmission system (Fig. 2) , comprising:

a transmitting circuit (the output driver 212) for transmitting out a signal (the signal to the bus 205);

a transmission line (the bus 205) for transmitting the signal output from the transmitting circuit;

a receiving circuit (the circuit 260) for receiving the signal transmitted from the transmitting circuit through the transmission line 205; and

a termination resistor circuit (the circuit 242) connected to the transmission line wherein the termination resistor (Fig. 5) comprises:

a first termination resistor block (the first block comprises transistors 542 and 544) having a plurality of transistors (transistors 542 and 544, i.e., more than one), the limitation that a gate of at least one of the transistors of the first termination resistor block being applied with a supply voltage or a voltage of the transmission line is met because the line 524 which is connected to the gates of transistors 542 and 544 can receive any voltage which includes the voltage of the supply voltage or a voltage of the transmission line; and

a second termination resistor block (the second block comprises transistors 560 and 532) having a plurality of transistors (transistors 560 and 532) with different logic voltages being applied to gates of the transistors (the logic voltage applied on line 528 to the gate of transistor 560 can be different from the logic voltage applied on line 526 to the gate of transistor 532), which differs in configuration from the first termination resistor block (transistor 560 is NMOS and transistor 532 is PMOS whereas transistors 542 and 544 are PMOSs, i.e., different configurations);

the limitation recited on the last two lines is met because they are controlled by different control signals.

As per claim 13, this claim is rejected for the same reason noted in claim 4.

As per claim 14, Ilkbahar discloses a signal transmission system (Fig. 2) , comprising:

a transmitting circuit (the output driver 212) for transmitting output a signal (the signal to the bus 205);

a transmission line (the bus 205) for transmitting the signal output from the transmitting circuit;

a receiving circuit (the circuit 260) for receiving the signal transmitted from the transmitting circuit through the transmission line 205; and

a termination resistor circuit (the circuit 242) connected to the transmission line wherein the termination resistor (Fig. 5) comprises:

a first termination resistor block (the first block comprises transistors 542 and 544) having a plurality of transistors (transistors 542 and 544, i.e., more than one) of the same conductivity type (both are PMOS); and

a second termination resistor block (the second block comprises transistors 560 and 532) having a plurality of transistors (transistors 560 and 532), which differs in configuration from the first termination resistor block (transistor 560 is NMOS and transistor 532 is PMOS whereas transistors 542 and 544 are PMOSs, i.e., different configurations);

the limitation that the first termination resistor block operates and maintains a specific resistance value when a value of the transmission line is near a supply voltage is met because

when the voltage applied to the gates of transistors 542 and 544 is unchanged when a value of the transmission line is near a supply voltage, the transistors 542 and 544 has a specific resistance value;

the limitation that the second termination resistor block comprises a first conductivity type and a second conductivity type reads on transistor 560 (PMOS) and transistor 532(NMOS), respectively, the limitation that the first conductivity type transistor does not operate near a first supply voltage and the second conductivity type transistor does not operate near a second supply voltage is met because transistors 560 and 532 have the structure which can perform the recited function; and

the limitation recited on the last two lines is met because they are controlled by different control signals.

As per claims 15 and 17, these claims are rejected for the same reasons noted in claims 6 and 8, respectively.

As per claim 18, this claim is rejected for the same reason noted in claim 9.

As per claim 19, this claim is rejected for the same reasons noted in claim 1, and further, the recited signal transmission system is disclosed in Fig, 2, the recited transmission line reads on the bus 205, the recited receiving circuit reads on the circuit inside the circuit 260 which receives the signal transmitted on the bus 205, and the recited termination resistor circuit reads on the circuit 242 which is provided in the interface circuit 240.

As per claims 20-22, these claims are rejected for the same reasons noted in claims 2-4, respectively.

As per claim 23, this claim is rejected for the same reasons noted in claim 1, and further, the recited signal transmission system is disclosed in Fig. 2, the recited transmitting circuit reads on the output driver 212, the recited transmission line reads on the bus 205, the recited receiving circuit reads on the circuit inside the circuit 260 which receives the signal transmitted on the bus 205 and the recited termination resistor circuit reads on the circuit 242 which is provided in the interface circuit 240.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,026,456 to Ilkbahar.

As per claim 7, Ilkbahar discloses a termination resistor circuit which comprises elements and connections as discussed in claim 4 above wherein each of the plurality of the second termination resistor blocks comprises third and fourth transistors having different conductivity type.

Ilkbahar does not explicitly teach that the third and fourth transistors are equal in size as called for in the claim.

However, choosing the size of transistors to obtain the optimized result in a circuit for a certain application in which the circuit has identical structure involves only routine experimentation, and is within the level of one skilled in the art. MPEP 2144.05.

It would have been obvious to one skilled in the art at the time of the invention was made to choose the size of the third and fourth transistors in the Ilkbahar's second termination resistor block to be the same.

The motivation/suggestion for doing so would have been obvious since it would have been easier to manufacture a lot of transistors having the same size than to manufacture a lot of transistors having different sizes.

As per claim 16, this claim is rejected for the same reason noted in claim 7.

Response to Arguments

7. Applicant's arguments filed 7/25/02 have been fully considered but they are not persuasive.

Regarding the argument that Ilkbahar fails to disclose or suggest a first termination resistor block having a plurality of transistors with a same logic voltage being applied to gates of the transistors and a second termination resistor block having a plurality of transistors with different logic voltages being applied and having different configuration from the first termination resistor block as recited in claims 1, 10, 19 and 23.

This argument is not found persuasive because it does not specify which element and/or connection which is recited in the claim and is not seen in the reference. As discussed in details in the preceding rejections, since each of recited element in the claim is seen in the Ilkbahar

reference, the claims are anticipated by the reference. In order for the argument to be found persuasive, the Applicant must be able to show which element and/or connection recited in the claim is missing in the reference. This argument fails to comply with 37 CFR 1.111(b) because it amounts to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the reference.

Regarding the argument that the reference fails to disclose or suggest a gate of at least one of the transistors of the first termination resistor block being applied with a supply voltage or a voltage of the transmission line as recited in claims 3, 12 and 21. The examiner notes that since transistor 542 in the first termination resistor block can receive a supply voltage or a voltage of the transmission line, the recited limitation is met. The examiner further notes that in a circuit claim, the manner of operating the circuit does not distinguish the claim from the prior art, i.e., a manner of applying the supply voltage or the voltage of the transmission line to the gate of the transistor in the first termination resistor block does not distinguish the claim from the reference since it does not result in a different structure. MPEP 2114.

Regarding the argument that the reference fails to disclose or suggest the first termination resistor block operates and maintains a specific resistance value when the signal of the transmission line is near a supply voltage. When the voltage on line 524 is unchanged when the signal of the transmission line is near a supply voltage, the specific resistance value of the first termination resistor block which comprises transistors 542 and 544 is defined.

Regarding the argument that the reference fails to disclose or suggest the second termination block comprises a first conductivity type transistor which does not operate near a first supply voltage and a second conductivity type transistor which does not operate near a

second supply voltage as recited in claims 5 and 14. Since transistor 560 is NMOS and transistor 532 is PMOS, by defining the first supply voltage is about 0 volt and the second supply voltage is about VT volts, the recited limitation is met, i.e., at about 0 volt, transistor 560 is OFF and at about VT volts, transistor 532 is OFF.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

MN
September 4, 2002